



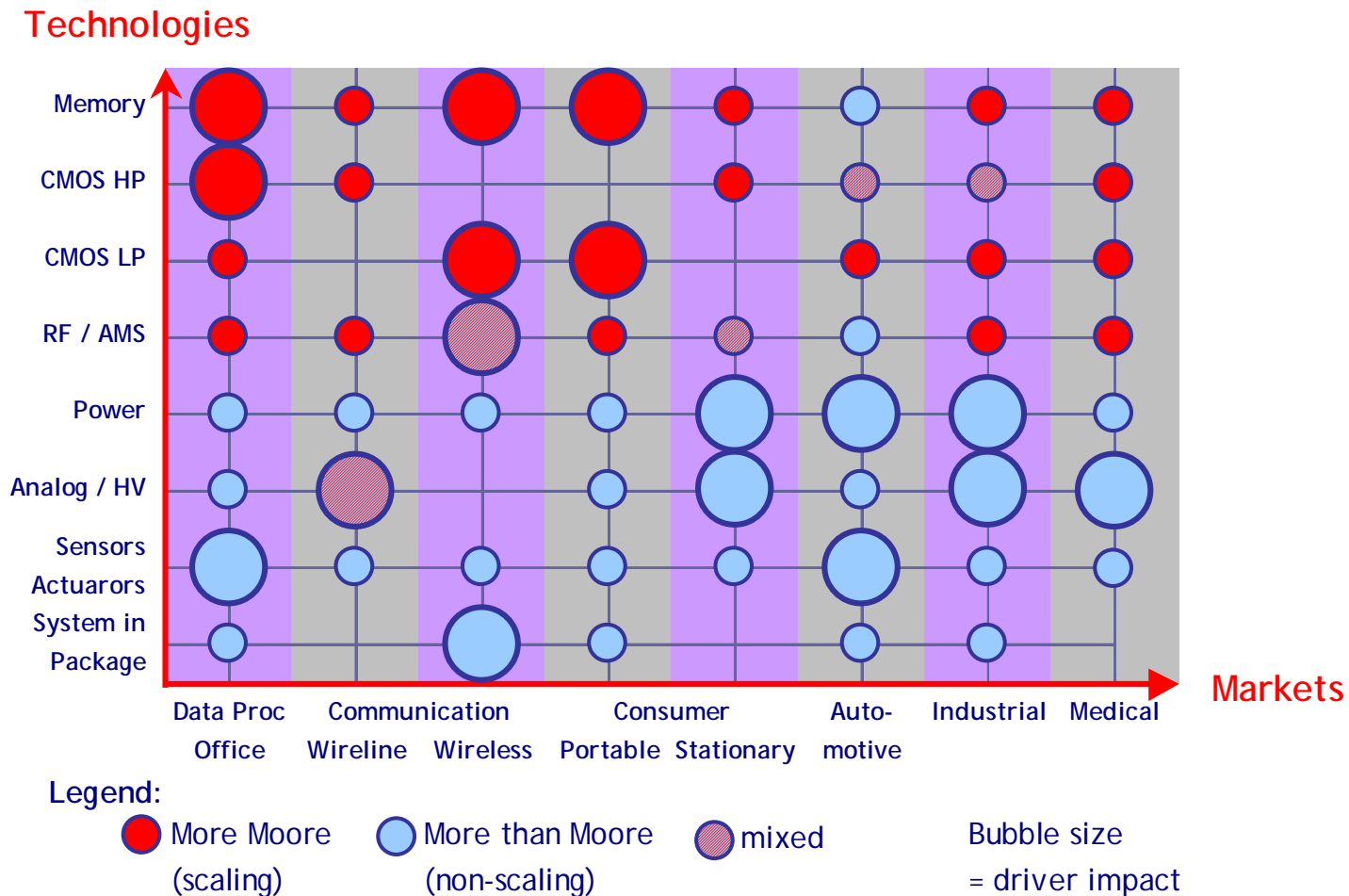
# ENIAC Joint Undertaking Multi-Annual Work Plan and Call 1 (2008)

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# Mapping technologies on markets (from Catrene White Book – Part B)



# Society needs (=applications) are leading

Health & wellness



Transport & mobility



Security & safety



Energy & environment



Communication



Infotainment

# Technological scope follows the ENIAC SRA

*JU Multi-annual Workplan*

More Moore

More than Moore

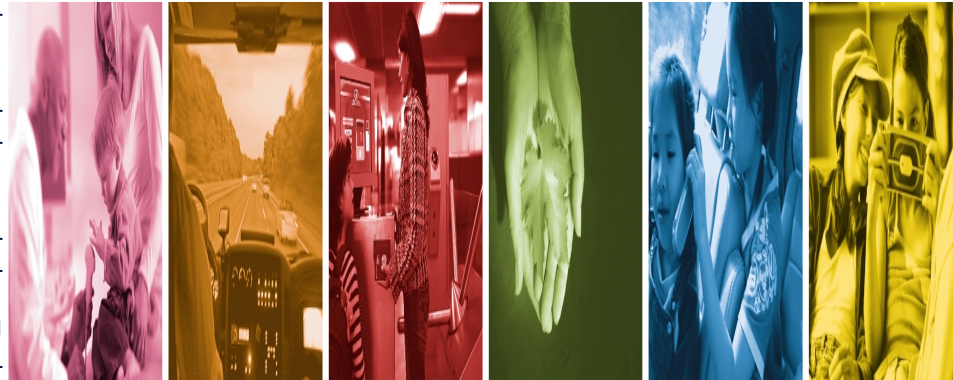
Heterogeneous Integration

Design Methods & Tools

Equipment & Materials

Beyond CMOS

Application programs 1 - 6



Generic platform 1

Generic platform 2

*Industry priorities for 2013 and beyond*



# Focus varies by application

Health & wellness

Transport & mobility

Security & safety



Energy & environment

Communication

Infotainment

*Favors More-than-Moore*

*Favors More Moore*

*Favors More Moore*

# JU topic mapping from the ENIAC SRA2007



# Health & wellness - JU topic mapping

- **Body sensors, wireless sensors, sensor networks and RF interfaces** for tele-monitoring
- **MEMS, NMEMS, bioMEMS and optical components**
- **Nanofluidic sampling and transport** for e.g. DNA/protein assay and automated drug-delivery
- **Bio-compatible and bio-resistant materials and packages** for portable / in-vitro and implantable / in-vivo applications
- **Ultra-low power technologies and design**, including **energy scavenging** systems
- **Extreme reliability, quality and test** on component and system level under harsh conditions (prediction, EMI, radiation, parasitics)

# Transport & mobility - JU topic mapping

- High performance **data processing** using **single- and multi-core components**
- **Smart power technologies** for energy management with **integrated processor, memory, power devices and sensors**
- **High power** technologies e.g. for Hybrid Cars based on **heterogeneous technologies** (e.g. Si, SOI, SiC, GaN )
- **Sensor and actuator** components and systems based on **heterogeneous substrates and functionalities** (e.g. Si, SiGe / RF, antennas, optical, energy scavenging)
- **Smart packages** and **high power modules** for heterogeneous integration with extended power dissipation
- **Reliability, quality and test** on component and system level under **harsh conditions** (prediction, EMI, radiation, parasitics)

# Security & safety - JU topic mapping

- Technologies for **trusted computing** and **privacy protection**
- **Specific memories** for codes and **encryption**
- New embedded **memories for smart cards**
- **Extremely cost efficient components** for “affordable security”
- **Power optimized technologies** for attack-resistant data processing
- Specific sensors for **recognition and identification** of individuals, of situations and of dangerous goods (e.g. camera modules, biometrical sensors, radar)
- Autonomous **sensing and communication networks**

# Energy & environment - JU topic mapping

- Highly cost-effective **wafer and chip HV-technologies** for improved breakdown / switching / frequency performance and device density
- New **materials and production technologies** for high power components (e.g. SiC, SOI, GaN, extreme wafer thinning) and new isolation techniques (e.g. selective SOI for HV)
- Innovative **silicon / package interconnection** technology for improved heat dissipation (e.g. thick Cu metallization)
- Highly efficient **thermal management** and cooling technologies
- **Heterogeneous integration on wafer and package** level of sensors, LED, controllers, filters, actuators and power devices
- **Innovative** system design and architecture for **(solid-state) lighting, AC/DC conversion** and **power drives**

# Communication - JU topic mapping

- Innovative **ultra-low power solutions**, including new materials, substrate engineering, digital error correction, and embedded PMUs / multicore architectures
- Platform-based technologies for highly efficient **system design up to 150 GHz**, including RFCMOS, BiCMOS, III-V and passives
- Low cost, low power solid state embedded and stand-alone **mass storage memory**
- **Analog / RF / HV** extensions at **65 nm and below**
- Cost-effective **SiP and SoC** co-optimization and design
- Assessment of the limits of classic interconnect schemes and **development of new interconnect technologies** (e.g. air gap, 3D, optoelectronic)

# Infotainment - JU topic mapping

- Technologies and devices for **ambient intelligence** environments and **human interaction**, including sensors and actuators such as MEMS and display drivers
- **Ultra low power** networks and devices
- High-density, **low power solid-state memories**
- Components for **high-speed data transmission, compression and storage** systems
- Technologies for **multi-format encoding / decoding, data distribution, and digital rights management**
- Technologies and devices for **image and sound capture**, analysis, **rendering**, and quality improvement

# Design methods & tools - JU topic mapping

- **Requirement mapping, modeling and engineering, and metrics** to measure and improve design productivity
- Constraint management and **unified design environment** for **IP-reuse** and on all levels of abstraction
- Modeling and simulation at high abstract level (hardware, software, environment), and **coherent integration** and implementation of **hardware and hardware-dependent software**
- Design for **reconfigurable systems**
- Design for **ultra low power**, design for **multi-core**, design for **RFCMOS**, and design for **Analog / Mixed Signal**
- Modeling, simulation, and physical models and efficient system level **co-design of heterogeneous systems** (board / chip / package)
- **Design for manufacturability**, design for yield, design for reliability, and design for test and analysis

# Equipment & materials - JU topic mapping

- High-quality **substrates and materials** for layer deposition, polishing and cleaning
- Advanced **lithography and metrology** system for large scale and flexible realization of nanometer-size geometries
- Advanced equipment for **layer deposition and etching**, thermal treatments, cleaning and process control
- Innovative tools, processes and materials for **packaging and final testing**
- Materials and process steps for eco-compatible and **sustainable manufacturing**
- Efficient, flexible, information-based manufacturing processes for **yield improvement and defect control**

# Organisation of the Joint Undertaking



- The ENIAC Joint Undertaking has been set up in February 2008
- It has held 3 Governing Board in order to adopt
  - Rules of operation and financial rules
  - Countries and EC approval on approach, **priorities, support and timing** in the Multi-annual Workplan
  - **Platforms and programs selected** into the first Annual Workplan
  - Integrate all building blocks and launch the **First Call**
- Interim staffing is ensured by European Commission, permanent staffing in progress during 2008
- AENEAS will provide support for the first call

# Implementation in the first Annual Workplan

- The **Annual Workplan** is a subset of the Multi-annual Workplan
- Targeting **vertically integrated projects** leading to representative **demonstrators**, covering at least one cross-functional platform and one key application
- Selection of topics in consultation with countries, EC, and other ETPs using the following criteria
  - Industry urgency
  - Synergy with other JTIs (ARTEMIS, Innovative Medicine, Clean Sky) and platforms (EPoSS)
  - Alignment with PA support

# The first Annual Workplan (first Call, in 2008)

- The 2 generic platforms
  - Equipment & Materials
  - Design methods & tools
- 3 application programs:
  - Energy & environment
  - Transport & Mobility
  - Security & safety



2007

Strategic  
Research  
Agenda

European Nanoelectronics Initiative Advisory Council

  
Strategic Research Agenda



# National Commitments to Call 1

- Total funding (EC + Member States) = €90 M

